CLAIMS:

1. Integrated circuit having a plurality of processing modules (M, S) and an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a packet based communication based on transactions between said plurality of processing modules (M, S), wherein each packet comprises a first predetermined number of subsequent words each having a second predetermined number of bits, wherein a first of said plurality of processing modules (M) issues a transaction by sending at least one packet over said interconnect means to a second of said plurality of processing modules (S), comprising:

- at least one packet inspecting unit (PIU) for inspecting bits of said at least one packet to determine bits not required for said issued transaction and for matching said not required bits of said at least one inspected packet with other bits of the same packet.

2. Integrated circuit according to claim 1, wherein said at least one packet inspecting unit (PIU) is adapted to match said not required bits with previous or following bits in the same packet.

3. Integrated circuit according to claim 2, wherein said at least one packet inspecting unit (PIU) is further adapted to match said not required bits with corresponding bits in a previous or following word in the same packet.

4. Integrated circuit according to claim 2 or 3, further comprising:

- at least one network interface (NI) associated to said first of said plurality of processing modules (I) for controlling the communication between said first of said plurality of processing modules (I) and said interconnect means (N), wherein each of said at least one packet inspecting units (PIU) is arranged in one of said network interfaces (NI).

5. Method for packet switching control in an integrated circuit having a plurality of processing modules (M, S) and an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a packet based communication based on transactions between said plurality of processing modules (M, S), wherein each packet

comprises a first predetermined number of subsequent words each having a second predetermined number of bits, wherein a first of said plurality of processing modules (M) issues a transaction by sending at least one packet over said interconnect means to a second of said plurality of processing modules (S), comprising the steps of:

- inspecting bits of said at least one packet to determine bits not required for the issued transaction and matching said not required bits of said at least one inspected packet with other bits of the same packet.